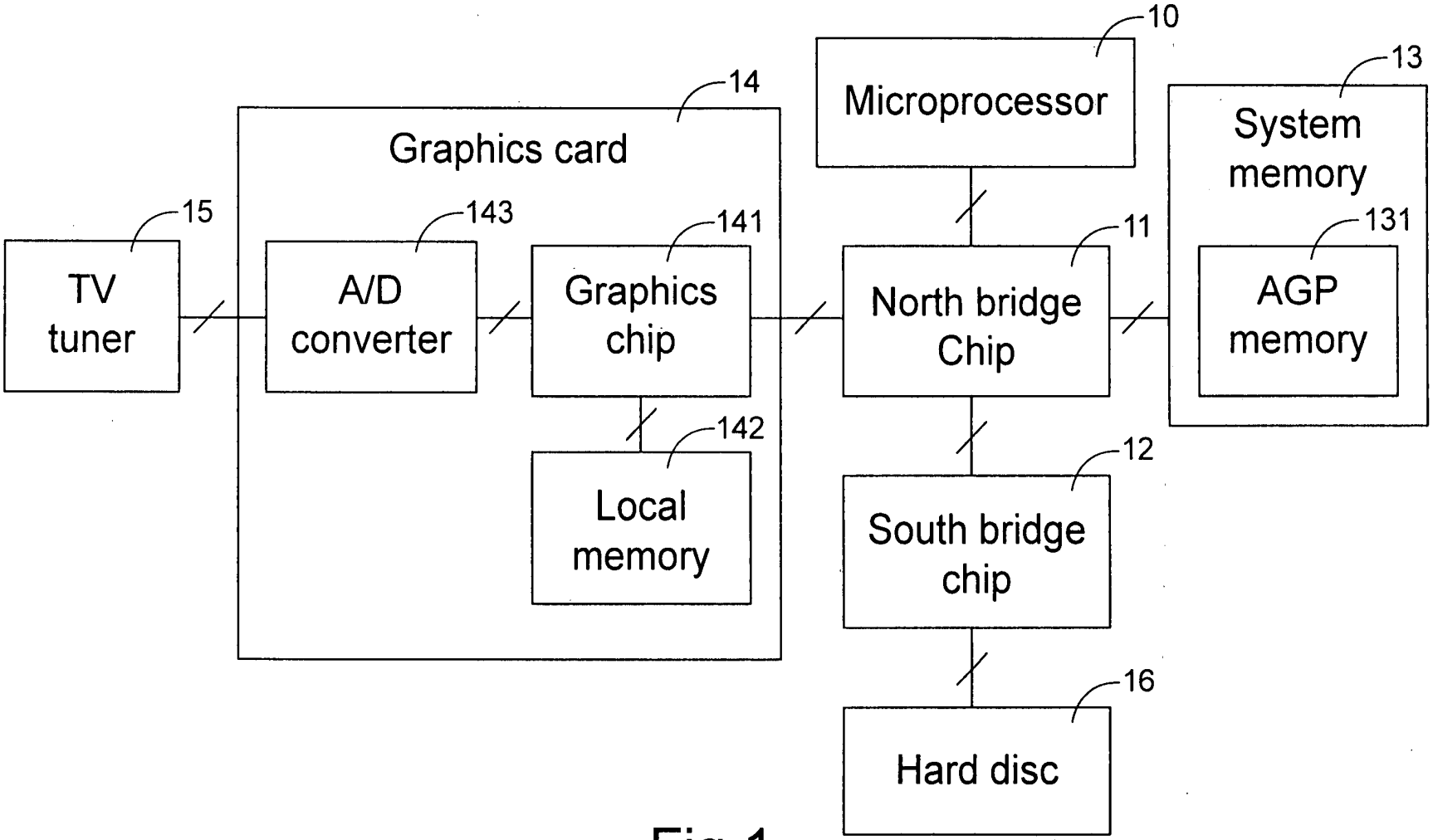

Fig.1
PRIOR ART

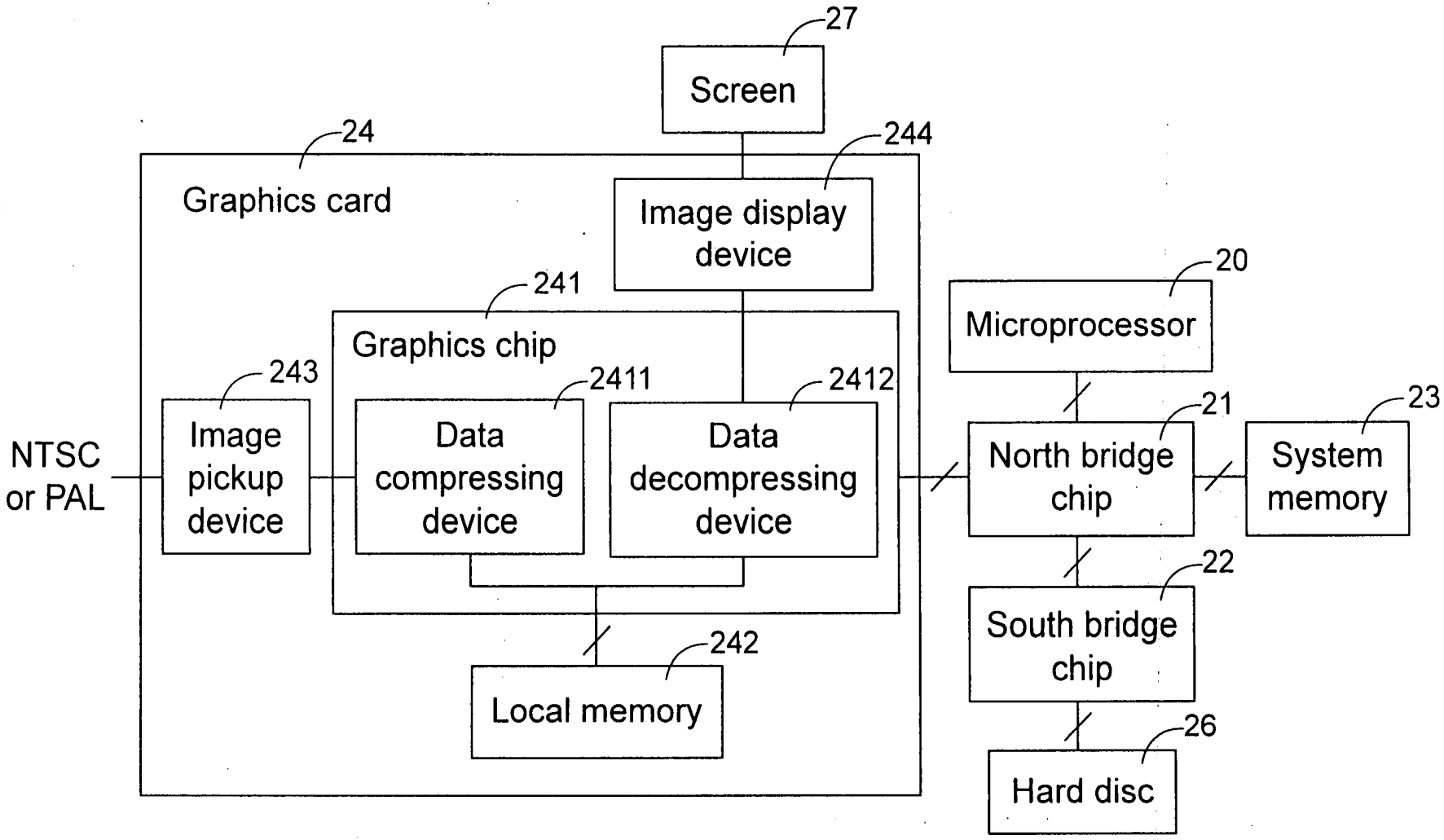
27
Screen
24
Graphics card
244
Image display device
241
Graphics chip
20
Microprocessor
243
2411
2412
NTSC or PAL
Image pickup device
Data compressing device
Data decompressing device
21
North bridge chip
23
System memory
22
South bridge chip
242
Local memory
26
Hard disc

Fig.2

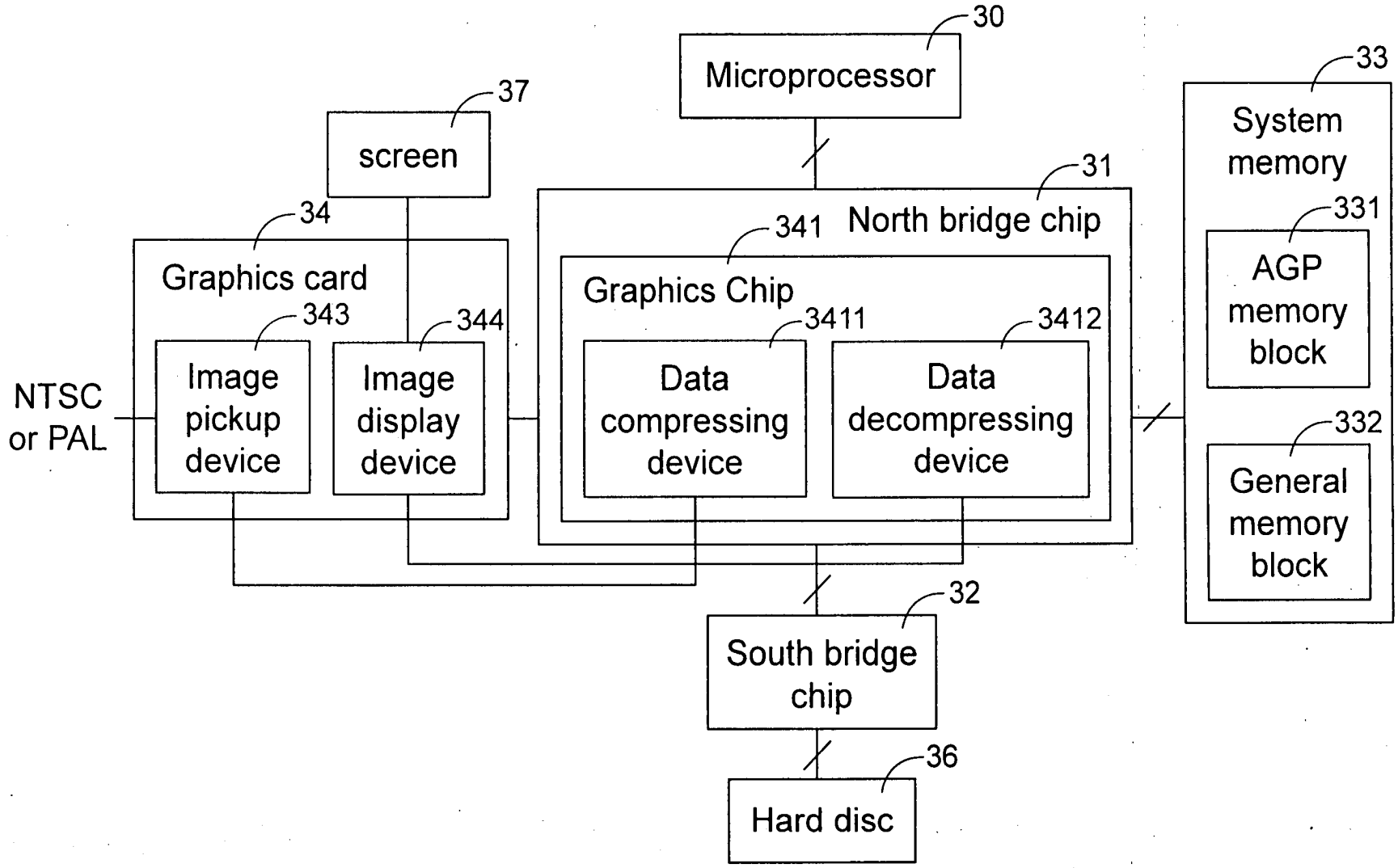
30
Microprocessor
37
screen
33
System memory
31
North bridge chip
34
341
Graphics card
Graphics Chip
331
AGP memory block
343
344
3411
3412
NTSC or PAL
Image pickup device
Image display device
Data compressing device
Data decompressing device
332
General memory block
32
South bridge chip
36
Hard disc

Fig.3

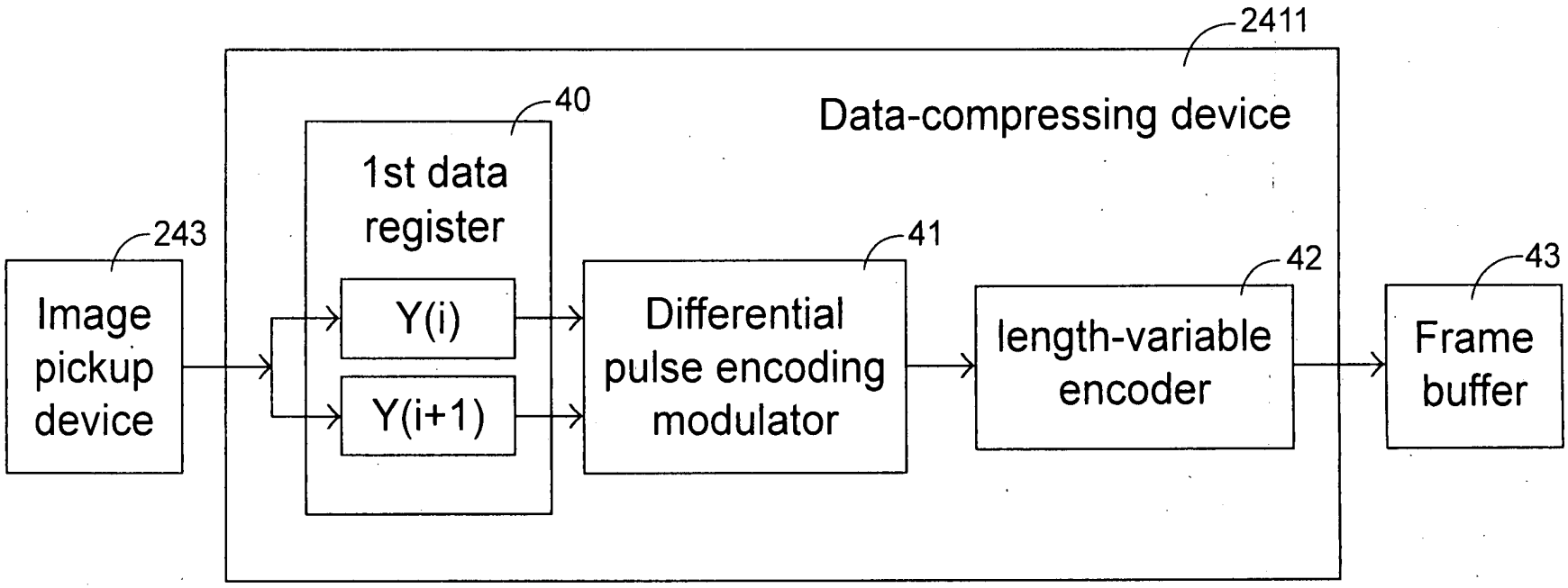
2411
Data-compressing device
40
1st data register
Y(i)
Y(i+1)
243
Image pickup device
41
Differential pulse encoding modulator
42
length-variable encoder
43
Frame buffer

Fig.4

Compression Decompression

Di=Y(i+1)[7:0]-Y(i)[7:0]	Recovery data code	Y'(i+1)
0	100	Y'(i)[7:0]
±1	101 s	Y'(i)[7:0]±1
±2	11 00 s	Y'(i)±2
±3	11 010 s	Y'(i)±3
±4	11 011 s	Y'(i)±4
±5	111 00 s	Y'(i)±5
±6	111 010 s	Y'(i)±6
±7	111 011 s	Y'(i)±7
±8	1111 000 s	Y'(i)±8
±9	1111 001 s	Y'(i)±9
±10	1111 010 s	Y'(i)±10
±11	1111 011 s	Y'(i)±11
±12	1111 100 s	Y'(i)±12
±13	1111 101 s	Y'(i)±13
±14	1111 110 s	Y'(i)±14
±15	1111 111 s	Y'(i)±15
Otherwise	Di/2	Y'(i) [7:0]+Di'

Fig.5A

	Compression	Decompression
Di=Y(i+1)[7:0]-Y(i)[7:0]	Recovery data code	Y'(i+1)
0	100	Y'(i)[7:0]
±1	101 s	Y'(i)[7:0]±1
±2	11 00 s	Y'(i)±2
±3	11 010 s	Y'(i)±3
±4	11 011 s	Y'(i)±4
±5	111 00 s	Y'(i)±5
±6	111 010 s	Y'(i)±6
±7	111 011 s	Y'(i)±7
±8	1111 000 s	Y'(i)±8
±9	1111 001 s	Y'(i)±9
±10	1111 010 s	Y'(i)±10
±11	1111 011 s	Y'(i)±11
±12	1111 100 s	Y'(i)±12
±13	1111 101 s	Y'(i)±13
±14	1111 110 s	Y'(i)±14
±15	1111 111 s	Y'(i)±15
Otherwise	0 Y(i+1) [7:1]	Y(i+1) [7:1] 0

Fig.5B

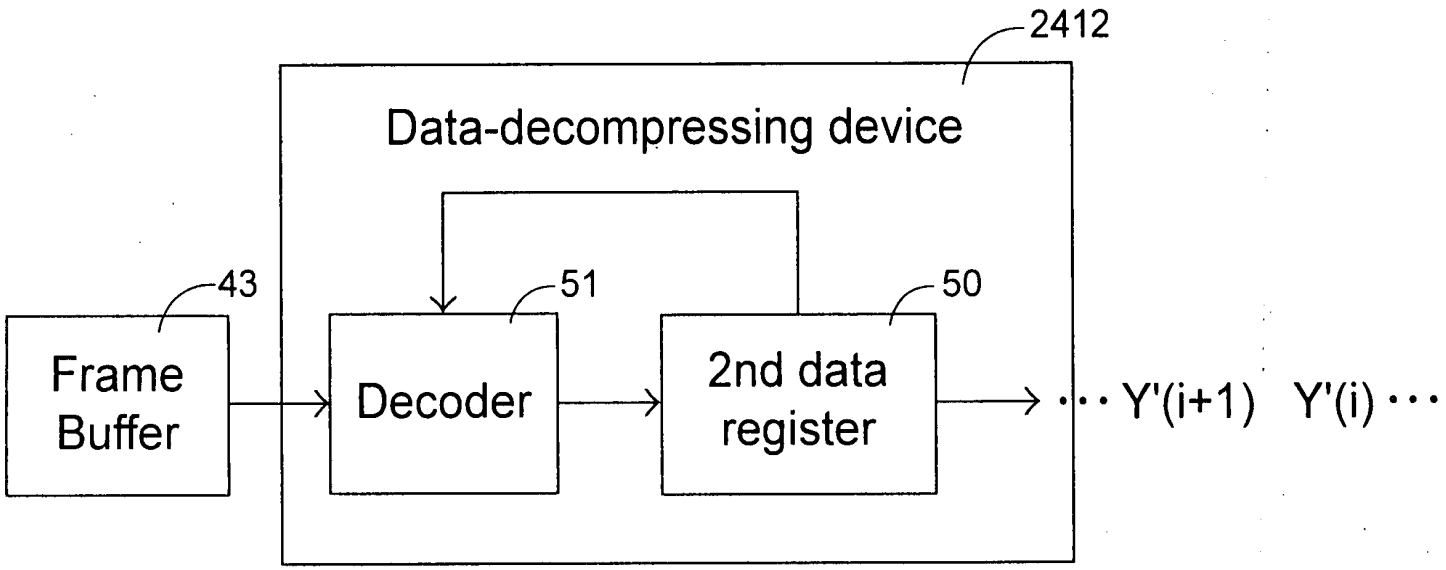
2412
Data-decompressing device
43
51
50
Frame Buffer
Decoder
2nd data register
Y'(i+1)
Y'(i)

Fig.6

Y	U	Y	V	Y	U	Y	V	Y	U	Y	V	.....
Y	U	Y	V	Y	U	Y	V	Y	U	Y	V	.....
Y	U	Y	V	Y	U	Y	V	Y	U	Y	V	.....
Y	U	Y	V	Y	U	Y	V	Y	U	Y	V	.....
Y	U	Y	V	Y	U	Y	V	Y	U	Y	V	.....

Fig.7A
PRIOR ART

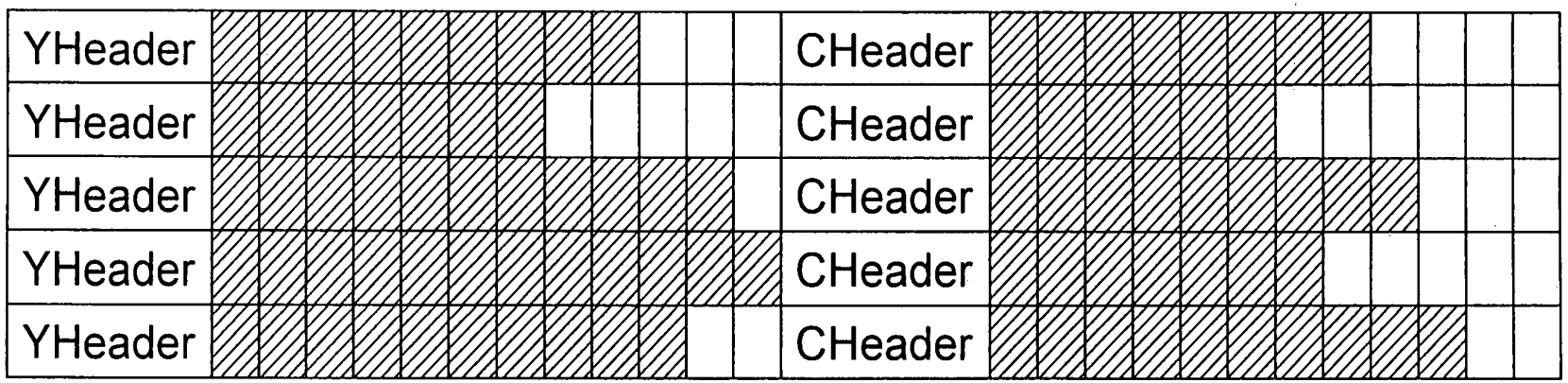

Fig.7B